Code.No: 43216 | R07 | SET-2

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
II.B.TECH - I SEMESTER REGULAR EXAMINATIONS NOVEMBER, 2009
DIGITAL LOGIC DESIGN
(Common to CSE, IT, CSS)

Time: 3hours **Max.Marks:80**

Answer any FIVE questions
All questions carry equal marks

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1. a) Write the number from 0 to 9 in any three 4 bit self complementing codes.
   b) Perform the following arithmetic operation on unsigned binary number.
   i) 11010-1101 ii) 101011-100110 (use 2's complement)
   c) What is the grays code equivalent of HEX number 47A, 331 H. [16]

2. a) List out the postulates used in Boolean algebra
   b) Obtain the canonical sum of product form of
   i) f = $\overline{A}BC + \overline{B}\overline{C}(A + D)$
   ii) f = $A(C + \overline{D}) + B\overline{C}$
   c) What is meant by weighted code. Give an example for weighted code and non-weighted code. [16]

3. a) Simply the following using K-maps.
   $f(A,B,C,D) = \sum(0,1,4,5,7,8,10,13) + \phi\sum(2,6)$
   b) Realize the above circuit using only NAND gates. [8+8]

4. a) Design a 4 bit carry look ahead adder circuit.
   b) Write HDL program to model the above adder in structure modeling style. [8+8]

5. a) Draw a neat circuit diagram of a negatives edge triggered JK flip flop and explain its operation.
   b) What is race around condition? How is it achieved is master slave flip-flops.[8+8]

6. Design an universal shift register of 4-bit. Explain each register operation with a waveform. Use JK flip flops in the design. [8+8]

7. a) Design a code converts circuit which converts Gray code to BCD using PALS.
   b) Design a combinational circuit which cubes the 3 bit binary input data. [8+8]

8. Obtain the flow table of a circuit with two input x_1 *and* x_2 and has two outputs Z_1 and Z_2 . $Z_1Z_2 = 00$ When $x_1x_2 = 00$; $Z_1Z_2 = 01$ when $x_1 = 1$ and x_2 changes from 0 to 1; $Z_1Z_2 = 10$ when $x_2 = 1$ and x_1 changes from 0 to 1; otherwise the output does not changes. [16]

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